Driving of I²S Bus Components with Audio Analyzer UPD

Application Note 1GA25_1E

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Subject to change

Products:

Audio Analyzer UPD

ROHDE&SCHWARZ

1. Summary

In contrast to standardized digital interfaces which are customary for communication between audio devices, diverse data formats are used between the internal modules of a particular device. The I²S interface developed by Philips has now been widely adopted for the latter.
The data structure of this digital audio interface and the adaptation of Audio Analyzer UPD in the different operating modes of the I²S bus are described in this Application Note.

2. Introduction

Standardized interfaces are nowadays used as a matter of fact for interconnecting digital audio equipment. In the professional field, the AES/EBU format has been widely adopted, while consumer units use the S/P DIF interface. Looking at the interconnection of the individual modules and components inside such audio equipment, however, reveals very individual and manufacturer-specific solutions.
A few years ago, Philips set themselves the target to standardize the interconnection of the individual digital components. To this end, a serial data bus was developed which meanwhile has been patented under the designation I²S bus (inter-IC sound bus) and adopted for use worldwide. Through the use of this data format it has become possible to integrate digital audio components from different manufacturers in one and the same equipment. Typical components are for instance A/D and D/A converters, digital signal processors and filter circuits, or integrated circuits which contain the entire audio processing for TV sets, car radios, etc.

To be able to carry out measurements on any type of digital interface, Audio Analyzer UPD has been equipped with programmable serial digital interfaces which allow practically any configuration regarding bit clock and word clock, word length, number of audio bits, bit sequence and word offset. Practically all data formats up to 1 MHz sampling rate can thus be adapted. This Application Note describes the wiring of the generator and analyzer interfaces in I²S format as one of the possible applications.

3. The Inter-IC Sound Bus (I²S Bus)

The inter-IC sound bus has been developed by Philips to enable the interconnection of audio ICs from different manufacturers. This bus system is used by many IC manufacturers today and is a patent of Philips.
The exclusive aim of this development was the connection of digital audio signals rather than the connection of control or error correction data which is not supported by this bus.

To keep the number of connecting lines low, a serial bus with three lines was selected, consisting of a data line (data) transmitting two data channels in time multiplex, a clock line (clock) and a channel select signal (word select).

In the simplest case, the transmitter chip generates clock, word select and data. In more complex systems with several transmitters and receivers it may be difficult to determine the master. To ensure errorfree data transmission in this case it is necessary to centrally generate the system clock and word select signal and to synchronize all chips accordingly. The master clock can be generated by a separate clock generator or by any of the chips involved. This means that both transmitter ICs and receiver ICs must be able to operate as slave. Moreover, there may also be applications in which a receiver IC operates as a master. The switchover between master and slave operation is software-controlled or by appropriate pin assignment.

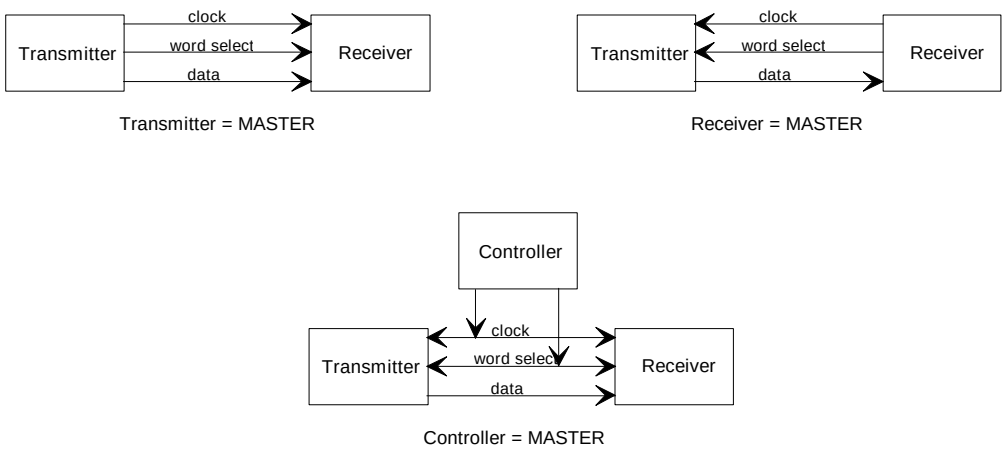

Fig. 1: I²S bus wiring diagram

The data signals are transmitted in two's complement beginning with the MSB. By starting with the MSB it is possible to interconnect chips with are able to process different word lengths. If more bits are sent than the receiver can process, the data words in the receiver are cut off; if words are received which are shorter than the internal word length of the receiver chip, zero bits are added. This shortening or filling up with zero bits is always made at the least significant bit. The position of the MSB in the data stream is defined by the word select signal, the LSB results from the internally available word length. The chip with the shortest word length thus determines the word length of the total system.

The polarity of the word select signal defines the data channel, word select = 0 marks channel 1 (left), word select = 1 marks channel 2 (right).

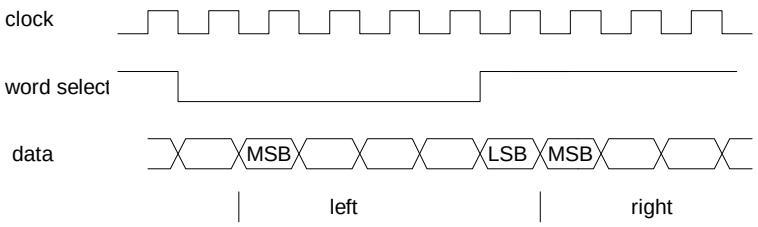

Fig. 2: Data structure and channel definition (timing for receiver chip)

4. Timing and Levels in I²S Bus

One chip in the system generates the master clock, while all other chips derive their internal clocks from this signal available at the clock input. All times defined in the specification of the I²S bus refer to a clock period of the system so that the clock frequency actually used is independent of this specification.

The transmitter chip always sends the data bits upon the falling edge of the clock signal. The receiver reads the data bits upon the rising edge of the clock, thus allowing sufficient settling time for the data bits. Although data transfer by the transmitter upon the rising clock edge is also possible if the timing of the chips allows reliable synchronization, it is hardly ever employed in practice.

The master chip transmits the word select signal upon the rising or falling clock edge, in any case one clock period before the MSB is sent (see Fig. 2). The word select signal is read into the receiver chips upon the rising edge of the clock signal. The receiver thus has sufficient time to store the previous data word and to reset its input.

The levels for the I²S bus format are specified for standard TTL components. It is however also possible to use other levels for driving new component families.

5. Digital Universal Interfaces of Audio Analyzer UPD

Before describing the different settings of Audio Analyzer UPD in the various wiring configurations of the I²S bus, some information about the basic capabilities of the UPD is to be given first. Audio Analyzer UPD features universal parallel and serial digital interfaces which can be configured for the generator and the analyzer section. The interfaces are also able to handle dual-channel audio signals which are either applied simultaneously to the different lines or processed successively in multiplex mode as required for operation of the I²S bus. Like with the I²S bus, clock line, data line and word select line are available at the serial universal interfaces; the pin assignment for generator and analyzer is shown in the table below.

Generator			**Analyzer**	
Signal name	**Remarks**	**Pin**	**Signal name**	**Remarks**
GND OUT5V GND	5 V, 50 mA	7,8 12 1,2	GND OUT5V GND	5 V, 50 mA
Channel 1: SCLKA SDATAA SWSA	Channel 1, with SERIAL MUX 1 & 2: Output bit clock Output audio data Output sync pulse (word clock) with MUX word select	 9 10 11	Channel 1: SCLKA SDATAA SWSA	Channel 1, with SERIAL MUX 1 & 2: Input bit clock Input audio data Input sync pulse or word clock
Channel 2: SCLKB SDATAB SWSB	Channel 2: Output bit clock Output audio data Output sync pulse (word clock)	 15 14 13	Channel 2: SCLK SDATAB SWSB	Channel 2: Input bit clock Input audio data Input sync pulse
SCLKIN SWSOUT	Input external bit clock Output word select with SERIAL MUX (frequency = audio clock)	4 5 6	ACLKOUT SWSOUT	Output bit clock output (8- to 32-fold audio clock) Output audio clock

The generator can directly generate the standardized clock rates 32 kHz, 44.1 kHz and 48 kHz as well as multiples thereof. If an external clock signal is applied, UPD can generate data words with sampling rates from 100 Hz to 1 MHz.

The bit format can be set to "MSB first" or "LSB first", the word length is adjustable in steps up to a length of 28 bits. Synchronization with the data bits can be made on the rising or on the falling clock edge, the edge of the word select signal can be shifted relative to the first data bit as desired. Fig. 3 shows the timing of the serial interfaces with the parameters that are important for further settings. It shows the setting word offset = 0, ie the data bit is transferred with the next clock following the word clock edge.

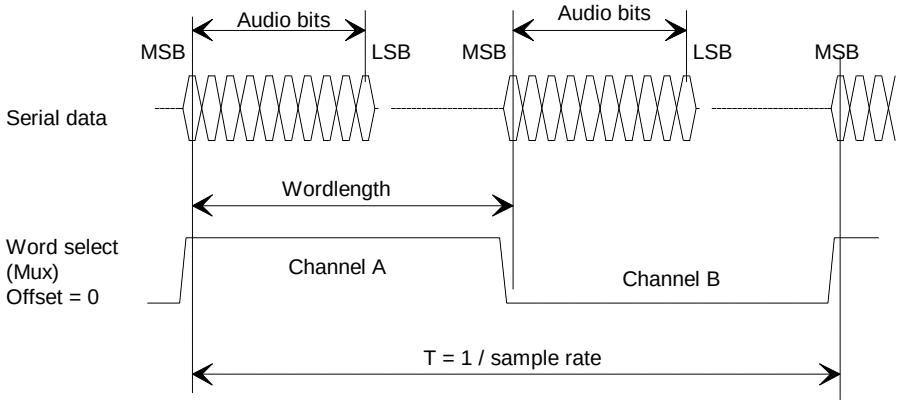

Fig. 3: Serial digital interfaces of Audio Analyzer UPD

With these comprehensive setting possibilities Audio Analyzer UPD covers practically all data formats occurring in practice. For the operation on I²S components the UPD must be configured according to the above specifications with due consideration given to the possible operating modes resulting from the master/slave definition.

6. Operating Modes for Measurements on the I²S Bus

Similar to the interconnection of I²S components, definitions have to be made when connecting the measuring instrument as to which chip or which part of the measuring instrument is to generate the clock and word select synchronization signals, ie assume the master function. The operating modes described under section 3 allow the following modes of interconnection with the Audio Analyzer UPD:

1. The UPD generator is master, while the UPD analyzer and all other components involved are slaves:
   This application is the normal case, in which Audio Analyzer UPD is used for measurements on a digital twoport. The generator of the UPD feeds all signals required to the receiver chip of the DUT. The device under test loops clock and word select signals through to its output and applies them to the analyzer input of the UPD.

2. Audio Analyzer UPD is exclusively used for analysis and as a master it must supply the clock and word select signals for the DUT.
   This for instance is the case if measurements have to be made on an A/D converter which must be synchronized to an external clock. The test signal is applied to the DUT in analog form, the analyzer measures the digital output data stream and thus operates as a slave.

3. The UPD generator operates as a slave:
   Application: The generator of the UPD supplies the digital test signals but is synchronized to a clock generated in the DUT. An example would be the measurement of a D/A converter which either generates the clock and word select signals itself or gets them from another clock generator in the DUT. This means that the generator of the UPD must be sychronized to the DUT.

7. Configuration of Audio Analyzer UPD in Generator = Master, Analyzer = Slave Mode

This operating mode is the standard case in the majority of all applications. Fig. 4 shows the cabling, with the generator of Audio Analyzer UPD operating as the master and generating the clock and word select signals as well as the digital audio data. The test signal passes through the receiver and transmitter stages of the device under test and the analyzer of the UPD is synchronized to the output signal of the DUT.
Based on this operating mode, the individual settings are described in detail in the following.

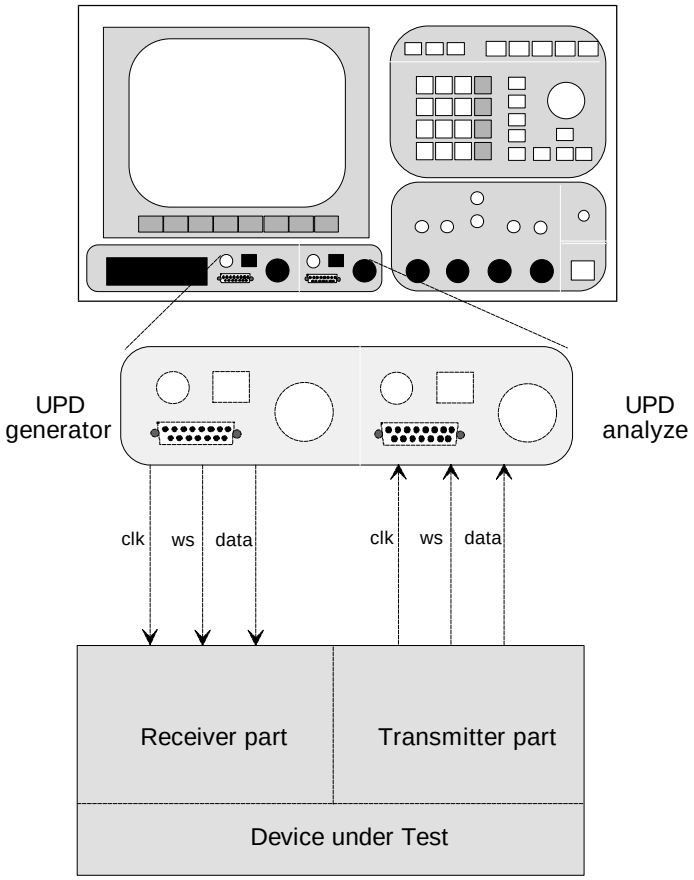

Fig. 4: Operation of Audio Analyzer UPD for measurements on I²S components

7.1. Basic Settings on UPD Generator

Selection of generator, *GENERATOR* menu item

For driving digital circuits, Audio Analyzer UPD has three generator units which differ in the maximum word clock frequency they can generate. These units are designated *DIG 48kHz*, *DIG 192kHz* and *DIG 768kHz* and are selected in the *GENERATOR* menu line. The *DIG 48kHz* and *DIG 192kHz* generators are solely suitable for driving I²S components, since only these units are able to generate dual-channel audio signals in multiplex mode.
For the majority of I²S applications ***DIG 48kHz*** is the right choice provided that the DUT need not be operated with clock rates above 48 kHz.

Selection of audio channels, *Channel(s)* menu item

With this menu item the user can choose whether only channel 1 or channel 2 is to contain audio data (the other channel containing zero bits only). If both channels are selected, generation of the audio data can be chosen to be in phase (*2 º 1*) or in phase opposition (*2 º -1*).
Usually, ***2 º 1*** is chosen.

Selection of output interface, *Output* menu item

For driving the I²S components, the serial interface on the UPD front panel is used. To configure this interface for dual-channel multiplex operation, the ***SERIAL MUX*** menu item must be selected.

Setting of sample frequency, *Sample Frq* and *Oversamp* menus

Audio Analyzer UPD generates the standard clock frequencies 32 kHz, 44.1 kHz and 48 kHz as well as (depending on the generator selected) the 2-fold, 4-fold, 8-fold and 16-fold frequencies thereof. The setting is made by selecting the desired basic frequency under *Sample Frq* and the oversampling factor under *Oversamp*. If for instance signals are to be generated with a clock frequency of 96 kHz, *48 kHz* with oversampling factor *2* must be selected.
If other clock rates are required, the UPD generator can also be synchronized to an external clock. For this purpose a clock signal (bit clock) of 100 Hz to 32 MHz max. is applied to the serial or parallel interface of the UPD. The maximum frequency of 1 MHz for the word clock applies to the *DIG 768kHz* generator, while for the *DIG 192kHz* generator the maximum frequency that can be processed is 300 kHz. In the *Sample Frq* menu the setting *EXTERN* must be selected for this operating mode. Moreover, the exact frequency of the word clock used [= bit clock / (2 x word length)] must be entered in the next menu item. This input is very important since the frequency entered here is used for calculation of the output data. If the entered frequency does not agree with the applied frequency, all generated signals will be frequency-shifted.
Usually, the standard frequencies are sufficient for testing the I²S components so that ***Sample Frq*** = ***48 kHz*** *and* ***Oversamp*** = ***1*** can be used as a standard setting.

Definition of word length in data stream, *Wordlength* and *Audio Bits* menu items

With the *Wordlength* menu item the number of bits of each data sample can be defined. Word lengths of 8 bits, 16 bits, 24 bits and 32 bits can be selected, in the last case only up to 28 bits being usable as data bits. The *Audio Bits* settings are closely related to the *Wordlength* settings. With the *Audio Bits* menu item the number of bits of the transferred data sample to contain audio data can be defined. It is for instance possible to generate in a 24-bit data stream audio data in CD player quality, ie to generate audio data with 16 bits only. The remaining bits are set to zero.
The settings in these two menu items must individually be adapted to the specific measurement application since both the ***Wordlength*** and the number of the ***Audio Bits*** **depend on the DUT.**

***Wordoffset* menu item**

This setting can be used to define the position of the sync pulses of the word select line relative to the beginning of the data words. The word select signal can be shifted over the total length of the data word. According to the timing specifications of the I²S bus the word select signal must change its polarity one clock period before the MSB, so that the correct setting on the UPD is ***Wordoffset*** = ***-1***.
In I²S applications, word lengths of 16 bits or 24 bits are normally used. In case of other word lengths, the UPD must be set to the next higher word length, with *Wordoffset* remaining set to *-1*, since according to definition the MSB will be sent first.

Definition of active clock edge, *Bitclock* menu item

The bit clock setting defines the polarity of the clock signal used to transfer the individual data bits. The standard setting for driving I²S components is ***FALLING*,** although output on the rising edge is allowed exceptionally by the Philips specification.

***WordselCh1* menu item**

The word select line carries a symmetrical squarewave signal with a frequency equal to the sample frequency. An audio channel is transmitted during each halfwave. The setting in the WordselCh1 menu item defines the channel and the halfwave of the word select signal during which this channel is output. This setting is defined for I²S applications, ie the UPD has to be set to ***WordselCh1* = *LOW.***

***Bit Order* menu item**

This setting influences the bit sequence in the data stream. For testing I²S components, ***MSB FIRST*** must be selected.

***Frq Bitclock* panel line**

This line in the UPD generator panel cannot be set by the user since it is a display panel providing information about the output bit clock. The bit clock is calculated from the word length set on the UPD, multiplied with the sample clock rate, times two for multiplex mode.

7.2. Basic Settings on UPD Analyzer

The settings on the analyzer largely corresponds to those on the generator, therefore only a few brief hints are given in the following:

Selection of analyzer instrument, *ANALYZER* menu item

The three analyzers *DIG 48kHz*, *DIG 192kHz* and *DIG 768kHz* differ in the maximum word clock frequency they are able to process. The *DIG 48kHz* and *DIG 192kHz* analyzers are solely suitable for measurements on I²S components, since only these units are able to analyze multiplexed dual-channel audio signals.
For the majority of I²S applications ***DIG 48kHz*** is the right choice provided that the DUT need not be operated with clock rates above 48 kHz.

Setting the lower frequency limit, *Min Freq* menu item

Depending on the selected analyzer unit, a lower frequency limit of 2 Hz, 10 Hz and 100 Hz can be set. When selecting AUTO or AUTOFAST, the measurement speed increases with increasing frequency limit. The usual setting is ***10 Hz***.

Selection of audio channels, *Channel(s)* menu item

With this menu item the user can choose whether channel 1, channel 2 or both audio channels are to be measured. Usually, ***BOTH*** is chosen.

Selection of input interface, *Input* menu item

SERIAL MUX has to be set for the measurement on I²S components.

Setting of sample frequency, *Sample Frq* and *Oversamp* menu items

For setting the sample frequency and the oversampling factor see the description for the generator unit. The analyzer always operates with the physically applied clock signal. For measurements on I²S components a maximum word clock frequency of 300 kHz is permitted when using the DIG192kHz analyzer.
If a sample frequency other than the standard clocks is used, this must be entered under VALUE. If the entered frequency does not agree with the applied frequency, all filter and frequency measurement results will be shifted accordingly.
The standard frequencies are usually sufficient for most applications of the I²S DUTs so that ***Sample Frq*** = ***48 kHz*** *and* ***Oversamp*** = ***1*** can be chosen as a standard setting.

Definition of word length in data stream, *Wordlength* and *Audio Bits* menu items

With the *Wordlength* menu item the number of bits of each data sample can be entered. With the *Audio Bits* menu item the number of bits of the transferred data samples that are to be used for the analysis can be defined. The remaining bits are cut off.
The settings in these two menu items must individually be adapted to the specific measurement application since both the ***Wordlength*** and the number of the ***Audio Bits*** **depend on the application.**

***Wordoffset* menu item**

The description for the generator section applies analogously.
The correct setting according to the timing specifications of the I²S bus is ***Wordoffset*** = ***-1***.

Definition of active clock edge, *Bitclock* menu item

The bit clock setting defines the polarity of the clock signal used to accept the individual data bits. ***RISING*** must be set in this case (in contrast to the generator setting).

***WordselCh1* and *Bit Order* menu items**

Same settings as for generator: ***WordselCh1*** = ***LOW*** and ***Bit Order*** = ***MSB FIRST***.

8. Configuration of Audio Analyzer UPD in Analyzer = Master Mode

8.1. UPD Used for Measurement Only

Possible applications of the UPD would be where the DUT is to be synchronized by the receiver (= Audio Analyzer) and the test signal is generated by another source, eg applied from a test CD. The test configuration already described will be used in this case, with the clock and word select signals supplied by the generator being taken to the synchronization inputs of the DUT. Fig. 5 shows such an application example.

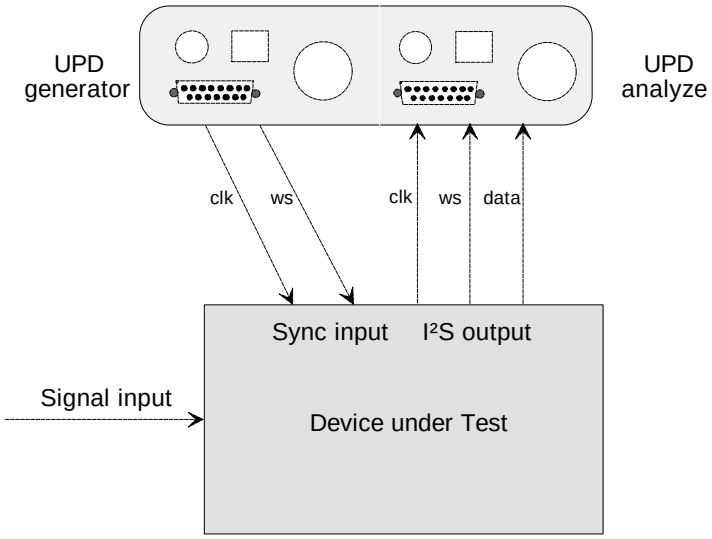

Fig. 5: Audio Analyzer UPD generating clock and word select

8.2. UPD Used for Measurement and Generation of Test Signals

For DUTs with analog inputs Audio Analyzer UPD not only performs digital measurements but also generates the analog test signals. The generator is then however not available for the generation of synchronization signals. DUTs of this kind (eg A/D converters) either generate clock and word select signals themselves or obtain these signals from a controller circuit which is then also available for the measurements. The UPD can thus be used as described in section 7.2 Basic Settings on UPD Analyzer.

A somewhat unusual application would be that of Audio Analyzer UPD having to generate the synchronization signals, too. This is possible with the aid of some additional cabling, provided that the standard clock frequencies of 32 kHz, 44.1 kHz or 48 kHz are used. With these settings the clock frequency is generated by a crystal in the UPD analyzer and brought out at pin 4 of the serial interface (see pin assignment table in section 5). The word select signal is generated with the aid of an external flipflop. The required cabling is shown in Fig. 6. For this operating mode of the UPD analyzer the settings analyzer = *DIG 192kHz* and *Oversampling = 2* must be selected since otherwise the word select signal would be generated with half the frequency only. Due to these settings, all frequency measurement results are displayed by a factor of 2. If filters are to be used, they have to be set to the twofold frequency to compensate for this effect.

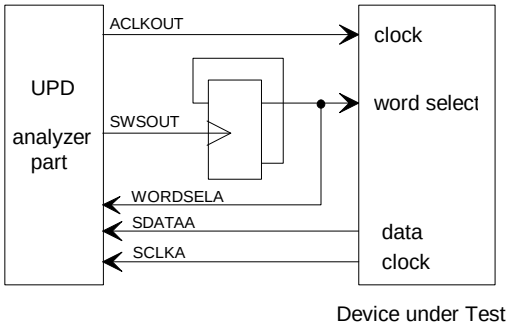

Fig. 6: Cabling for use of UPD analyzer as a master

9. Configuration of Audio Analyzer UPD in Generator = Slave Mode

This is not a very frequent application. A possible example would be the measurement on a D/A converter, with the clock and word select signals being generated by the DUT itself so that the test generator needs to be synchronized to the DUT. The clock signals may also be taken from a controller circuit as shown in Fig. 7.

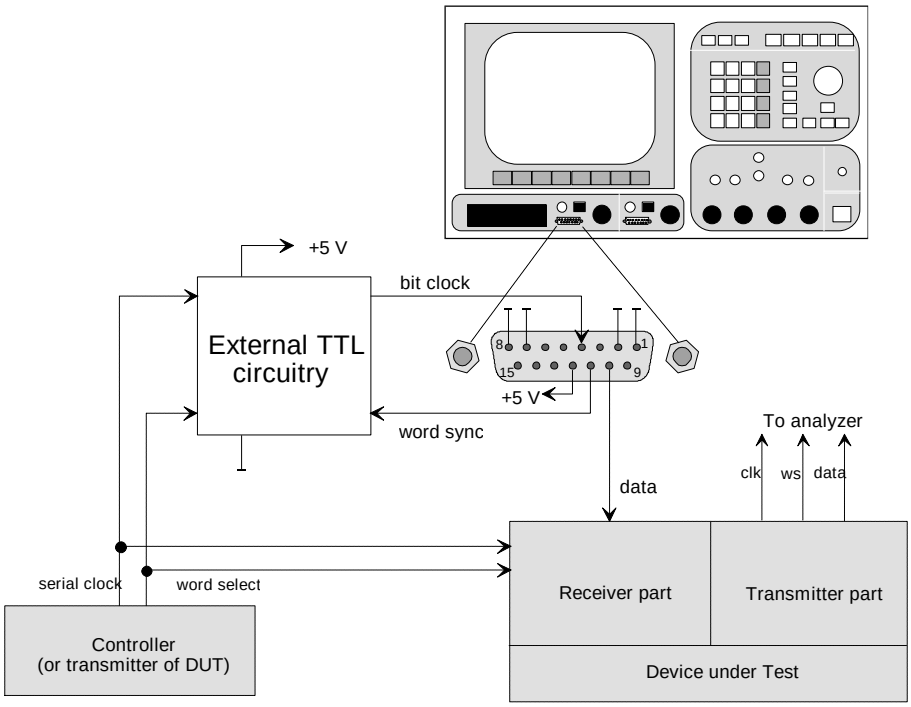

Fig. 7: UPD generator operating as a slave

This operating mode of Audio Analyzer UPD is also possible, the data generator must however be synchronized via an external circuit. The DUT or test setup must provide the system clock (bit clock) and the word clock while the UPD generates the data contents. Fig. 7 shows the test setup for this application. The external circuit generates the clock signal for the UPD from the two input signals. With this clock signal, data bits are output by the UPD, the number of bits per data word being defined in the generator panel. The word sync signal generated by the UPD is taken back to the external circuit for synchronization with the external word clock.

9.1. External Circuit

Fig. 8 shows the external circuit which is used to synchronize the UPD for the generation of data signals.

Any 5 V TTL logic components may be used for configuring this circuit. In the example shown a dual-D flipflop 74HCT74, a quad XOR gate 74HCT86 and a quad NOR gate 74HCT02 are used. This additional logic circuit is powered from the UPD. For this purpose a 5 V line is brought out at pin 12 of the serial output connector from which a current drain of 50 mA max. is available. The ground signal is present at pins 1, 2, 7 and 8 (see also Fig. 7).

The following input signals are required:

- System clock (bit clock) for output of the individual data bits. The UPD generator is able to process frequencies up to 32 MHz.
  Compared to a single-channel signal generation, the system clock must be greater by a factor of 2 for transmitting the same data word rate, since the data words for both channels have to be transmitted in the same time.
- Word clock, the rising edge of which defines the beginning of the data words.
- Bit clock and word clock must be synchronous.

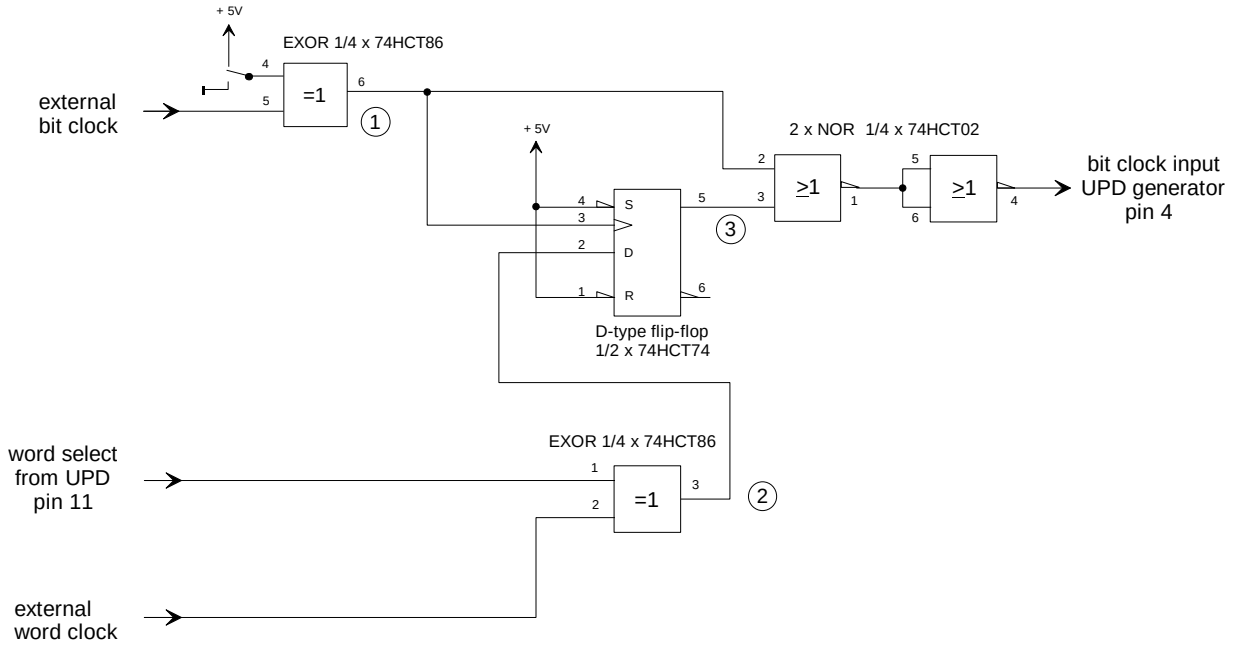

Fig. 8: External circuit of UPD data generator for external synchronization

If dual-channel signals are transmitted in multiplex mode, the word clock is a symmetrical squarewave signal with an audio channel being transmitted in each of its halfwaves. Since this applies both to the external signal and to the word select signal generated by the UPD, the external circuit may be quite simple.

9.2. Description of External Circuit for Synchronization of UPD

Fig. 9 shows the timing diagram. In the example shown, 8-bit data words are used which can be generated by the UPD in the minimum setting. This is a good example for describing the circuit.

Function of XOR gate at the input of the bit clock:

To ensure reliable switching conditions at any time, the rising edge of the word clock must be transferred upon the falling edge of the clock signal. If this is not possible with the given circuit of the application, the clock signal can be inverted with the aid of the XOR gate by connecting pin 4 to +5 V. In the other switching condition the clock signal passes the gate unchanged so that the gate would actually not be required.

Synchronization with word select signal of UPD:

The external word clock signal is compared in the XOR gate with the word select signal from the UPD. If the signals are identical, the output of gate is at low and a clock signal is applied to the UPD via the NOR gate as shown in Fig. 7 above. After switchover of the external word clock signal, a high signal is through-connected to the output of flipflop upon the next rising edge of the external clock signal on line ①. The following NOR gate is inhibited. Since there is now no clock signal, the output lines of the UPD remain unchanged. In the example shown the UPD stops upon output of data bit "7".
Switching the external word clock again enables the clock for the UPD, whereupon data bit "8" from channel A is output. This is the last data bit set in the UPD generator panel under *Wordlength = 8,* whereupon the UPD sets the word select line to high for the subsequent output of channel B. The bit clock signal at the output of the NOR gate is however interrupted again since the channel coding of the external word clock signal does not agree with that of the UPD. Subsequently, data will not be output.

Output of first synchronized data words:

The external word clock signal switches to "channel B" and thus agrees with the channel coding of the UPD. The next rising clock edge on line① switches the output of flipflop to low, the clock signal is passed on by the NOR gate and the UPD outputs the first data bit for channel B. Another seven data bits are output until the word length set in the generator panel is reached and the word select signal is switched to "channel A". The external word clock signal now also changes to low so that there is no change at output of the flipflop. The UPD now outputs eight data bits for channel A. This process is repeated for the second channel, the output of the first two data words for both channels is thus completed and the synchronization is locked.

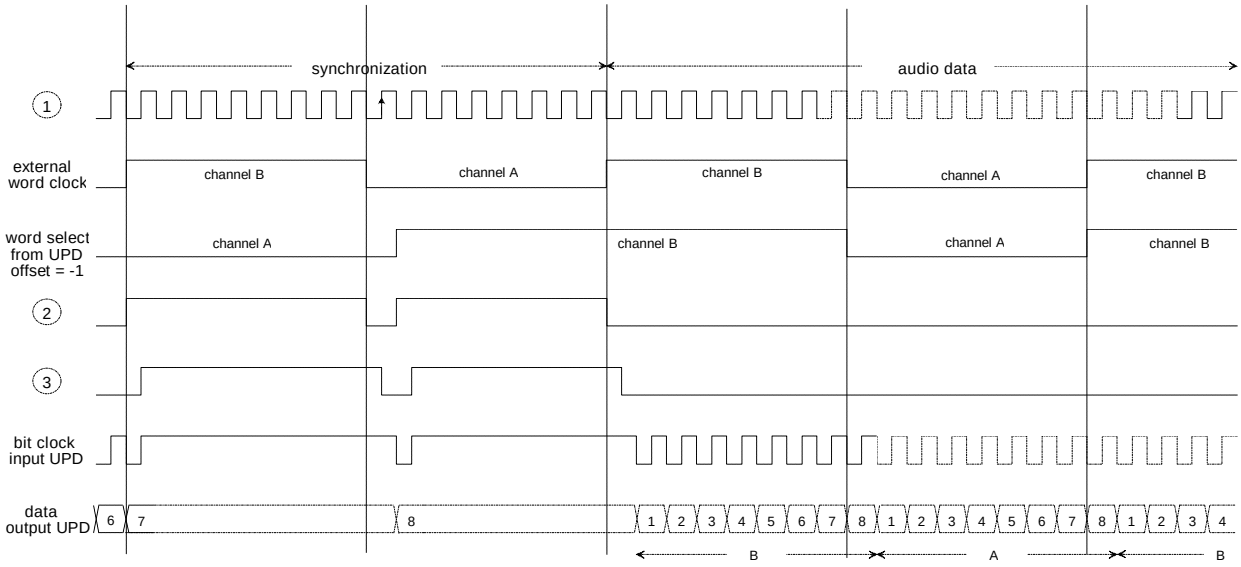

Fig. 9: Timing diagram for the generation of dual-channel multiplexed audio data

9.3. Settings on Audio Analyzer UPD

The basic generator settings have already been described in section 7.1. Therefore, the differences are briefly explained in the following. The following settings are to be made on the UPD generator:

Selection of generator, output channels and output interfaces

Set the ***GENERATOR*** to ***DIG 48kHz***, or to *DIG 192 kHz,* like in the other operating modes. For the channel selection, ***Channel(s)*** is usually to be set to ***2 º 1***. For dual-channel operation, the serial digital interface has to be set to ***SERIAL MUX.*** With the ***Sync To*** menu item the setting ***EXTERN*** must be selected for the synchronization.

Setting of sample frequency, *Sample Frq* and *Oversamp* menu items

For setting the sample frequency and the oversampling factor see the description of the generator settings in section 7.

Definition of word length in data stream, *Sample Freq* and *Oversamp* menu items

As already explained in section 7, the settings have to be adapted to the measurement application or device under test.

***Wordoffset* menu item**

In this circuit configuration, **Wordoffset must always be set to *-1*** since otherwise the beginning of the word would be shifted into the next or previous data word and the audio data thus split between two data words. The generated data signal is output with a word offset of 0. This corresponds to the I²S specification which defines that the word select signal is switched one clock period before the MSB.

***WordselCh1* and *Bitclock* menu items**

The setting under *WordselCh1* defines the halfwave of the symmetrical squarewave signal for the data output of channel 1. According to the definition for the I²S applications ***WordselCh1 = LOW*** has to be set.
The *Bitclock* setting is also defined in the I²S specifications. The data words must be transferred upon the falling edge of the clock signal applied to the UPD, ie ***FALLING*** is the default setting.

***Bit Order* menu item**

MSB FIRST is the correct setting for I²S applications.

Fig. 7 also shows the digital analysis of the audio signals from the DUT. The test configuration corresponds to that described in section 7, the analyzer operating as a slave and using serial input interfaces.
In the application described above, ie measurement of a D/A converter, the analysis would be carried out by the analog analyzer section of the UPD.

10. Driving D/A Converters with a Multiple of the Clock Frequency

It often occurs in practice that D/A converters have to be driven which, in addition to the clock, word select and data lines, have an input to which a multiple of the clock frequency has to be applied. This clock is used for internal signal processing in the converter, eg to implement filters. The 128-fold or 256-fold clock frequency are frequently used in this case.

Apart from the bit clock, the generator of Audio Analyzer UPD cannot generate any other clock signals. If however a multiple of the clock frequency is available together with the word select signal from an external circuit, the UPD can be operated similar as in the example described above.

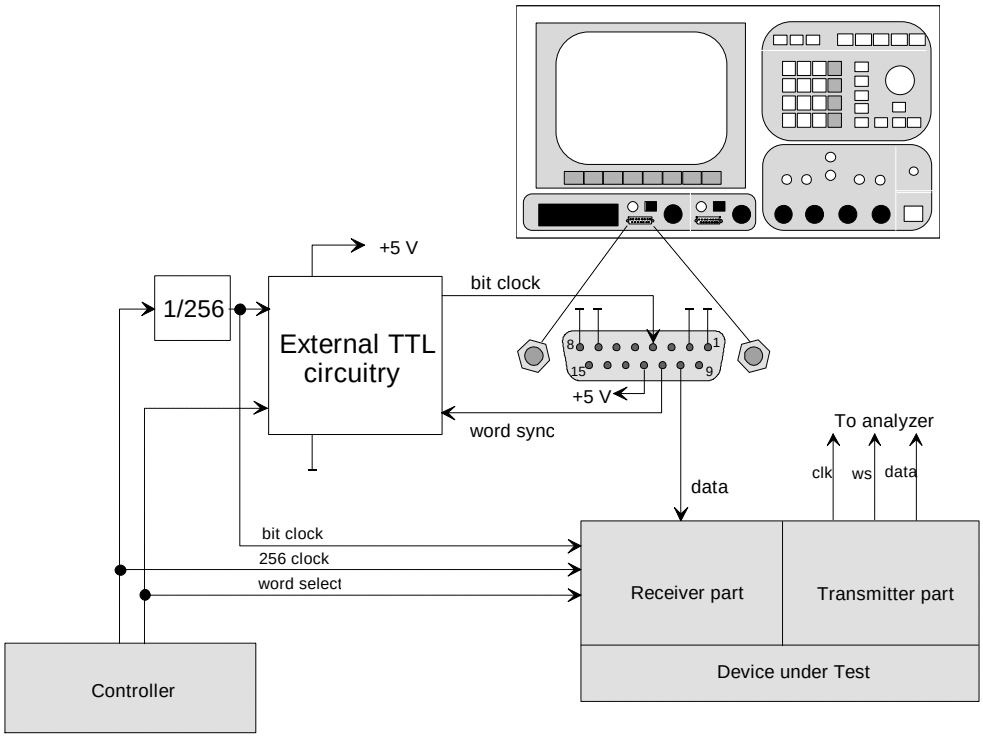

Fig. 10: Synchronization circuit with a divider added

The generator of Audio Analyzer UPD is thus synchronized to the external signals as described in detail in section 9. A divider has to be added to the circuit shown in Fig. 8, which divides the externally multiplied clock down to the bit clock of the I²S data stream used in the UPD for the data output. All necessary settings were described in the previous section.

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